DELHI COLLEGE OF TECHNOLOGY& MANAGEMENT (DCTM),PALWAL	**INSTRUCTION PLAN**	**RECORD NO.: QF/ACD/01 Revision No.: 00**

Name of Faculty: **SWATI** Department: **ECE/CSE**
Course Title: **DIGITAL SYSTEM DESIGN** Course Number: **EE-330-F**
Semester/Section: **6th SEM ECE** Session: **JAN – MAY 2018**

Instruction Plan Details:

Lecture No.	Topics to be covered	References
1	**SECTION-A:** Introduction to Combinational & Sequential circuits, Computer-aided design tools for digital systems. Hardware description languages;	BHASKER, Shipra Gupta, Yogesh Mishra
2	introduction to VHDL	-do-
3	Explanation of Identifiers, Data objects, classes	-do-
4	data types	-do-
5	Overloading, logical operators	-do-
6	**Problems on above**	
7	Types of delays	-do-
8	Entity declaration, Introduction to Package, Library, Generics	-do-
9	Introduction to behavioural ,dataflow and Structural models.	-do-
10	Examples of above models	
11	**SECTION-B** Behavioural Model: Assignment statements, sequential statements and process	-do-
12	**Problems on statements**	
13	Conditional statements, case statement with MUX.	-do-
14	Dataflow Model and related statements with MUX.	-do-
15	Cont –Dataflow Model with MUX.	
16	Modelling, component declaration, structural layout	-do-
17	Cont- Structural Model with MUX.	
18	Array and loops, resolution functions	-do-
	SECTION-C	

19	Packages and Libraries, Subprograms: Application of Functions and Procedures.	-do-
20	Designing of Encoders with all Models	-do-
21	Decoders	-do-
22	Code converters(BCD-7 segment)	
23	comparators, implementation of Boolean functions	-do-
24	VHDL Models of Sequential Circuits like Shift Registers (SISO)	-do-
25	Cont- SIPO, PIPO	-do-
26	VHDL Models of Counters	-do-
27.	VHDL models of Boolean equation	-do-
28	**SECTION-D** Basic components of a computer, specifications, architecture of a simple microcomputer system	-do-
29	implementation of a simple microcomputer system using VHDL Programmable logic devices : ROM	Gaganpreet Kaur
30	VHDL program for Memory subsystem,I/O Subsystem	Gaganpreet Kaur
31	VHDL for ALU.	Gaganpreet Kaur
32	Introduction to PLD and Types	Yogesh Mishra
33	PLD types cont(GAL,PEEL)	Yogesh Mishra
34	Design implementation using CPLDs and FPGAs	Yogesh Mishra
35	**Question Paper Discussion**	

NO. OF BOOKS AVAILABLE IN THE LIBRARY:

1. **J. Bhasker- 32**
2. **Shipra Gupta- 24**
3. **Yogesh Mishra- 28**

Signature of Faculty Member **HOD/Principal/Academic Coordinator**

Date